# High Precision Methodology Control for Nano MTJ Fabrication Process up to 150 mm Wafers

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## Abstract

Spintronic devices have received a great attention in the past decades, and provided considerable applications in industry and electronic information. Among them, one highlights the spin transfer torque magnetic random access memory (STT-MRAM), pointed as the next generation of non-volatile memory with commercialized products entering the market very soon, and the already mature HDD read heads already in sub 100 nm range. Still, current demands concerning stacking density, devices size and performance, continuously push the limits of standard nanofabrication techniques.

The basic building blocks of both structures is the magnetic tunnel junction (MTJ), which is a highly scalable technology. Scaling-down the MTJ critical features down to 30 nm and simultaneously integrate them on larger area wafers with highly controlled and standardized process, providing a very high yield of working devices, is a main challenge for magnetic storage industries nowadays. INESC-MN has already demonstrated successful patterning of nanoscale MTJs down to 100 nm based on a lift-off process with yield of 88% [1]. However, this progress was limited to 25 mm substrates. A more promising route towards sub 100 nm was also explored using chemical mechanical polishing (CMP). A 30 nm full MTJ device was demonstrated, although the process showed significant challenges in controlling the CMP end point reflecting dramatically in the final yield of working devices [2].

This work, relies on a distinct method for fabrication of sub 100 nm MTJ devices, targeting large yield in 150 mm substrates. Nano-MTJs were fabricated using combination of optical lithography (OL), ion milling and electron beam lithography (EBL). Then, to achieve functional and operational devices, the critical steps are the nanopillars definition and the definition (and opening) of electrical vias to pillars after passivation (300 nm $SiO_2$ film). The nanopillars (circles of 30 to 100nm diameter) are defined by EBL using a Raith-150 System and negative resist [3] followed by two-step ion milling etching, while the vias (500 nm size) are defined by EBL using a positive resist (PMMA) followed by Reactive Ion Etching (RIE) (see Figure 1).

Final yield of working devices depends on a large number of factors, such as resist and $SiO_2$ thickness and uniformity, exposure resolution and alignments, or RIE end-point and RIE uniformity. At this point, we focus on EBL. We have systematically studied the misalignment between consecutive write field (WF) exposures, stage movement drift and misalignment between BE, nanopillars and vias, critical for the success of the fabrication process on 150 mm wafers. Customized test structures were designed for automatic quantification of local deviations. Analyses were performed using SEM images, image process and data analysis programs (see Figure 2). Our results provided deviations between WF (of 500 µm) exposures up to 530 nm in the horizontal direction, and a maximum of 700 nm in the vertical direction. We also demonstrate highly uniform (better than +-1%) negative EBL resist coating up to 80 nm thick (see Figure 3) which provides the minimum resolution of our EBL system [2].Gathering all these factors, we can set a maximum value tolerance (~250 nm) for the misalignment of the mix & match exposure between BE, nanopillars and vias using a WF=500 µm for single isolated devices. This conditions are crucial in expediting a large yield MTJ nanofabrication process run for 150 mm wafers towards commercialization of nanodevices.

## References

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[2] R. Macedo, J. Borme, R. Ferreira et al., Journal of nanoscience and nanotechnology 10, **2010**, 1-7
[3] D. Leitão, R. Macedo, A. Silva et al., Proceedings of the IEEE Conference on Nanotechnology, **2012**

## Figures

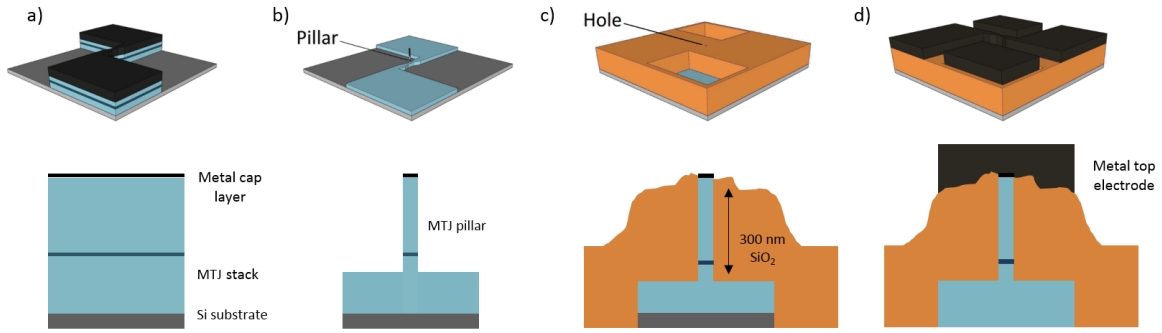


**Figure 1:** Illustration of the nano fabrication process from bottom electrode definition until metallization of top electrode (a)-(d), highlighting the critical steps of nanopillars definition (b) and definition and opening of electrical vias to pillars after passivation (c) . Top: 3D model of the fabrication process. Bottom: Section of the MTJ device during fabrication process.

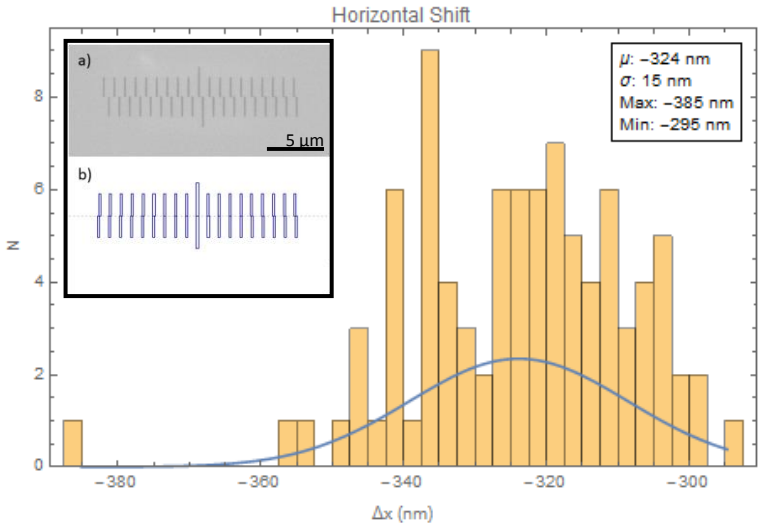


**Figure 2:** Statistical analysis of horizontal misalignment between consecutive write-fields exposures in a 20 x 20 $mm^2$ map on 150 mm wafer. The inset shows: a) SEM image of misaligned exposed structures and b) design of test structures for automatic quantification of local deviations

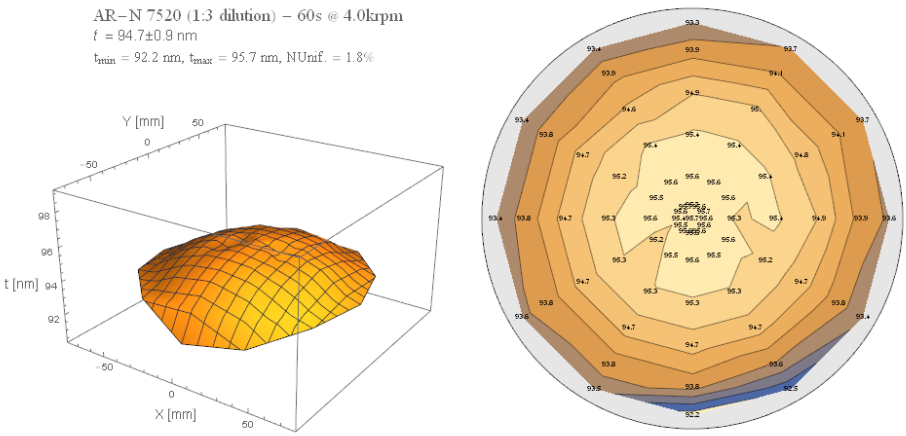


**Figure 3:** Left: 3D negative EBL resist profile thickness along a 150 mm wafer measured by ellipsometry; Right: Uniformity thickness profile of negative EBL resist