Vertical current in graphene – insulator/semiconductor – graphene structures

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Abstract
Two dimensional (2D) materials have emerged in the last decade [1] as a new route to engineer material properties, with an unmatched degree of tunability. Van der Waals (vdW) hybrid structures, formed by stacking different layers of 2D crystals on top of each other, are one of the most recent developments in the field of 2D materials [2]. Of particular relevance are the graphene – insulator/semiconductor – graphene structures, with hexagonal boron nitride/transition metal dichalcogenide playing the role of the insulator/semiconductor spacer. These structures have already been shown to operator both as a transistor (where the vertical current flowing between the two graphene layers is controlled by a gate voltage) [3] and as a photodetector [4].

Due to the atomically sharp nature of the interfaces between different layers in vdW structures, crystal momentum is conserved (modulo any combination of reciprocal lattice vectors). This fact, together with energy conservation, severely restricts the states which are coupled between different layers. As such, lattice alignment between different layers plays a fundamental role in the operation characteristics of graphene – insulator/semiconductor – graphene devices. In particular, lattice misalignment between the graphene layers has been shown to give origin to, and control, the occurrence of negative differential conductivity (NDC) [5,6].

In this work we perform a detailed study of the current characteristics of a graphene – insulator/semiconductor – graphene device as a function of the rotation angle between the insulator/semiconducting spacer and the graphene layers. We find out, that when this angle is very small, additional peaks in the current as a function of bias voltage appear, with several bias voltage windows displaying NDC. We also study the effect of disorder and phonons, which can transfer additional momentum to the tunneling electrons, in the vertical current between two graphene layers in graphene – insulator/semiconductor – graphene structures.

References
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[4] Britnell, L.; *et al*; Science **340** (2013) 1311 – 1341.

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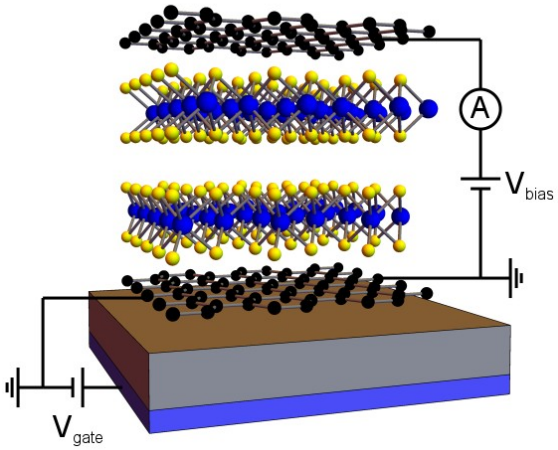
Figures

A



B

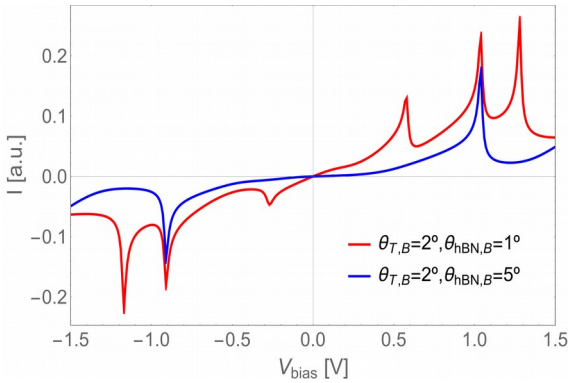


Figure 1 – (A) Schematic representation of a graphene – insulator/semiconductor – graphene device, indicating how the gate and bias voltages are applied. (B) I-V curve for a graphene – boron nitride – graphene device for a gate voltage of 40 V, with fixed angle between the top and bottom graphene layers (2º) and for two different rotation angles between the bottom graphene layer and the boron nitride spacer (1º and 5º). While for the larger rotation angle, only two peaks appear in the I-V curve, for the smaller angle additional peaks appear. This are related to the transference of momentum by the boron nitride lattice.