Fabrication of Nano-sized Magnetic Tunnel Junctions with features below 100 nm by Chemical Mechanical Polishing

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Abstract

Intense research regarding the development of magnetic tunnel junctions (MTJ) has been mostly driven by the magnetic data storage industry [1]. Nevertheless, MgO-based MTJs showing large tunnel magnetoresistance (TMR) are also expected to originate novel spintronic devices [2], such as MRAMs or nano-oscillators, where the targeted active area is typically below 100 nm. Therefore, a standard process to fabricate sub-micrometer pillar devices beyond lift-off based methods is crucial. In general, the fabrication of micrometric MTJ samples includes four steps: 1) definition of the bottom electrode (BE) area by optical lithography and ion milling etching; 2) junction area definition also by optical lithography and etching; 3) passivation by oxide, in order to prevent the electrical current from flowing between BE and top electrodes (TE) through anywhere else but the junction area and lift-off; and 4) the last step of the process is dedicated to the definition of TE by optical lithography, metallization and lift-off.

One of the critical issues arising from shrinking the junction area is related with the approach of establishing the electrical contact to the top of the nano-sized feature. Strategies, using a standard lift-off process [3, 4], are usually used. In the lift-off method, after the junction definition by electron-beam lithography (EBL) a passivation layer needs to be deposited on top for lateral insulation between BE and TE [3, 4, 5]. As the resist layer used for EBL is usually thin (hundreds nanometer thick), the oxide lift-off tends to be difficult. This process leads to residues from lift-off [3, 4], as shown in figures 1(a)-(b); the nanometric element can also be buried inside the passivation layer, as shown in figure 1(c). As a result, the fabrication of samples with features below 100 nm by lift-off is time consuming and has an extremely low yield.

To address this challenge, strategies of nano-fabrication processes using Chemical Mechanical Polishing (CMP) have been used for, since they are relatively simple and provide quick advantages. In the CMP-based nano-fabrication process, after the definition of the nanopillar, a thick SiO_2 (~ 200 nm) layer is deposited and then, CMP is used for planarization. The wafer is rotated under pressure against a polishing pad in the presence of a water-based solution containing very fine suspended abrasive particles (slurry), as shown in figure 2. In this work, we use 20 N as working pressure between sample and pad, a head and base velocity of 50 rpm, and a rate of slurry dispensing of 55 mL/min, leading to a polishing rate of 2.4 nm/min. This polishing rate is suitable to control the CMP end point in an accurate way, avoiding damage the top part of the nanopillars. To monitor the CMP process we use profilometer measurements, optical inspection and electrical measurements.

Using this technique, we remove the oxide layer down to the top of the MTJ pillars, allowing electrical contact to the top electrode. This allows a more efficient process for nano-sized magnetic tunnel junctions for features below 100 nm and with a reduced process time.

References

[1] P.P. Freitas, et al. J. Phys.-Cond. Mat. 19, (2007), pp. 165221

[2] W. Shen, X Liu, D. Mazumdar and G. Xiao, Appl. Phys. Lett. 86, (2005), 253901

[3] A.V. Silva, D.C. Leitao, Z. Hou, R.J. Macedo, R. Ferreira, E. Paz, F.L. Deepak, S. Cardoso, P. P. Freitas, IEEE Transactions on Magnetics, 49, (2013), pp. 4405 – 4408

[4] D.C. Leitao, Macedo, R.J. Silva, A.V. Hoang, D.Q. MacLaren, D.A. McVitie, S. Cardoso, P.P. Freitas, IEEE-NANO., (2012), DOI: 10.1109/NANO.2012.6321945

[5] R. Macedo, J. Borme, R. Ferreira, S. Cardoso, P. P. Freitas, B. Mendis and M. MacKenzie, J Nanosc. Nanotech., vol. 10, (2010), pp. 5951-5957

Figures

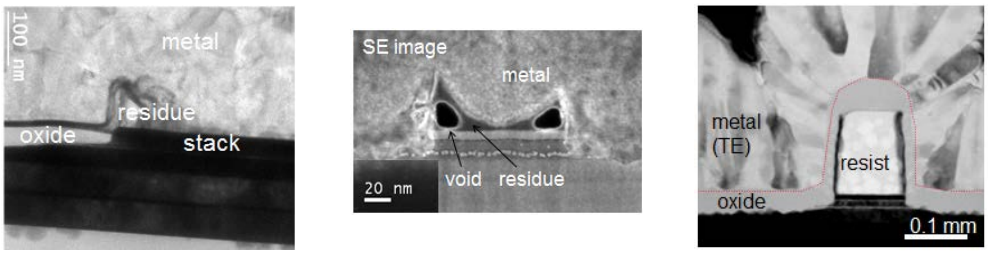

Fig. 1: (a) Nanopillar with lift-off residue along the pillars boundary; (b) Nanodevice with voids in TE, lift-off-based process failed [5]; (c) Nanodevice with resist buried inside oxide lag [5].

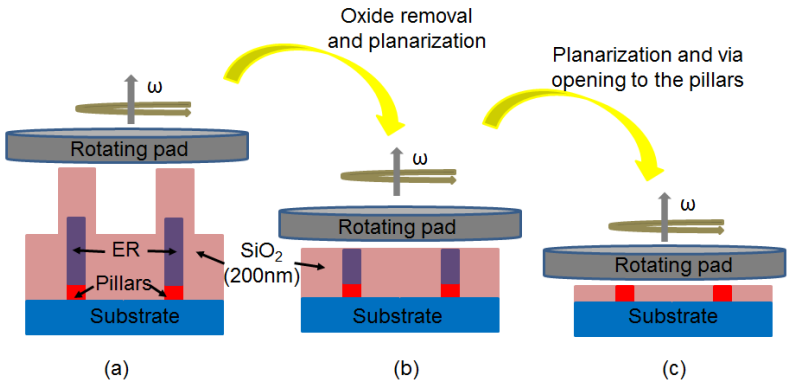

Fig. 2: The schematic diagram of CMP-based nano-fabrication process.